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United States Patent [19]

Nevill

[11] **Patent Number:** **6,021,265**[45] **Date of Patent:** ***Feb. 1, 2000****[54] INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS****[75] Inventor:** Edward Colles Nevill, Cambridge, United Kingdom**[73] Assignee:** ARM Limited, Cambridge, United Kingdom

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

This patent is subject to a terminal disclaimer.

[21] Appl. No.: 08/840,557**[22] Filed:** Apr. 14, 1997**Related U.S. Application Data****[62]** Division of application No. 08/477,781, Jun. 7, 1995, Pat. No. 5,758,115.**[30] Foreign Application Priority Data**

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[51] Int. Cl.⁷ G06F 9/30**[52] U.S. Cl.** 395/385; 395/386**[58] Field of Search** 395/384, 385, 395/386**[56] References Cited****U.S. PATENT DOCUMENTS**

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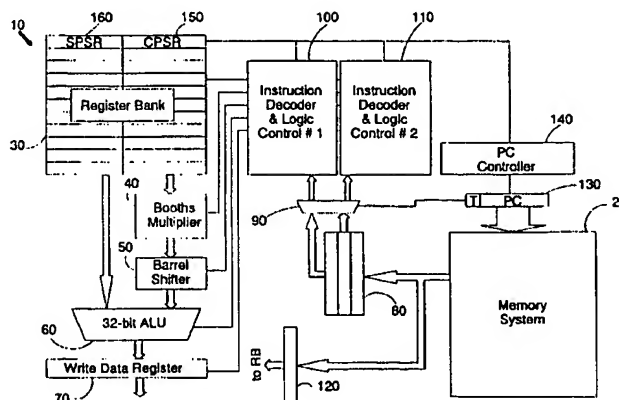
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Primary Examiner—Robert B. Harrell**Assistant Examiner**—Kenneth R. Coulter**Attorney, Agent, or Firm**—Fenwick & West LLP**[57]****ABSTRACT**

Data processing apparatus comprising: a processor core having means for executing successive program instruction words of a predetermined plurality of instruction sets; a data memory for storing program instruction words to be executed; a program counter register for indicating the address of a next program instruction word in the data memory; means for modifying the contents of the program counter register in response to a current program instruction word; and control means, responsive to one or more predetermined indicator bits of the program counter register, for controlling the processor core to execute program instruction words of a current instruction set selected from the predetermined plurality of instruction sets and specified by the state of the one or more indicator bits of the program counter register.

14 Claims, 3 Drawing Sheets

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